Name & Std. No.: Wyatt Duberstein 629635057 Lab Section: 19

Date: 11/18/2020

**Submission Instructions:**

**Prelab:**

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

**Lab:**

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

**PRELAB:**

*Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.*

**Q1.** Design a simple counting device (Section 2.0).

Number of States: 6

Number of State Variables: 6

**State Table: State-Assigned Table:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | Next State | | Output |  | Present State | Next State | | Output |
| w=0 | w=1 |  | w=0 | w=1 |  |
| A | A | B | A |  | 000 | 000 | 001 | 000 |
| B | B | C | B |  | 001 | 001 | 010 | 001 |
| C | C | D | C |  | 010 | 010 | 011 | 010 |
| D | D | E | D |  | 011 | 011 | 100 | 011 |
| E | E | F | E |  | 100 | 100 | 101 | 100 |
| F | F | A | F |  | 101 | 101 | 000 | 101 |

Canonical SOP Expressions for Next State Logic:

Y0 = w’y0 + wy0’

Y1 = w’y1 + y1y0’ + wy0y1’

Y2 = w’y2 + y0’y2 + y1’y2 + wy0y1y2’

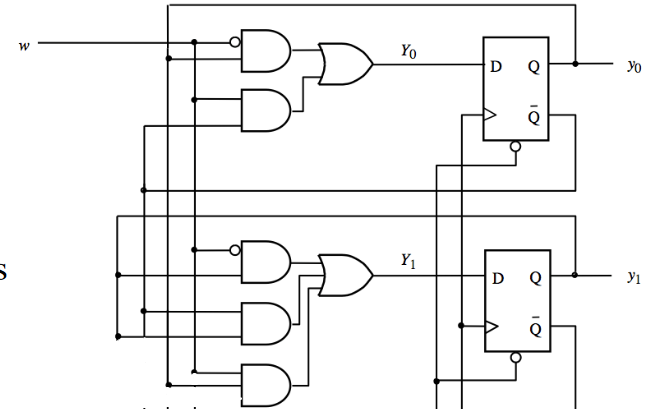
Simplified Next State Logic Expressions:

Y0 = w’y0 + wy0’

Y1 = w’y1 + y1y0’ + wy0y1’

Y2 = w’y2 + y0’y2 + y1’y2 + wy0y1y2’

Circuit Diagram:



**Q2.** Design a simple counter (Section 3.0).

Number of States: 4

Number of State Variables: 4

**State Table: State-Assigned Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| A | A | B | 0 |
| B | B | C | 2 |
| C | C | D | 4 |
| D | D | A | 5 |

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| 000 | 000 | 010 | 000 |
| 010 | 010 | 100 | 010 |
| 100 | 100 | 101 | 100 |
| 101 | 101 | 000 | 101 |

Canonical SOP Expressions for Next State Logic:

Y0 = y2

Y1 = wy2y1y0 + w’y1

Y2 = wy1 + y2

Simplified Logic Expressions:

Y0 = y2

Y1 = wy2y1y0 + w’y1

Y2 = wy1 + y2

Next State Logic Verilog Code:

module circuit\_nsl(w, Q1, Q0, Y1, Y0);

input w, Y2, Y1, Y0;

output Q2, Q1, Q0;

assign Q0 = Y2;

assign Q1 = (w & Y2 & Y1 & Y0) | (~w & Y1);

assign Q2 = (w & Y1) | Y2;

endmodule

Output Logic Verilog Code:

module circuit\_ol(Q1, Q0, Z2, Z1, Z0);

input w, Y2, Y1, Y0;

output Q2, Q1, Q0;

assign Q0 = Y2;

assign Q1 = (w & Y2 & Y1 & Y0) | (~w & Y1);

assign Q2 = (w & Y1) | Y2;

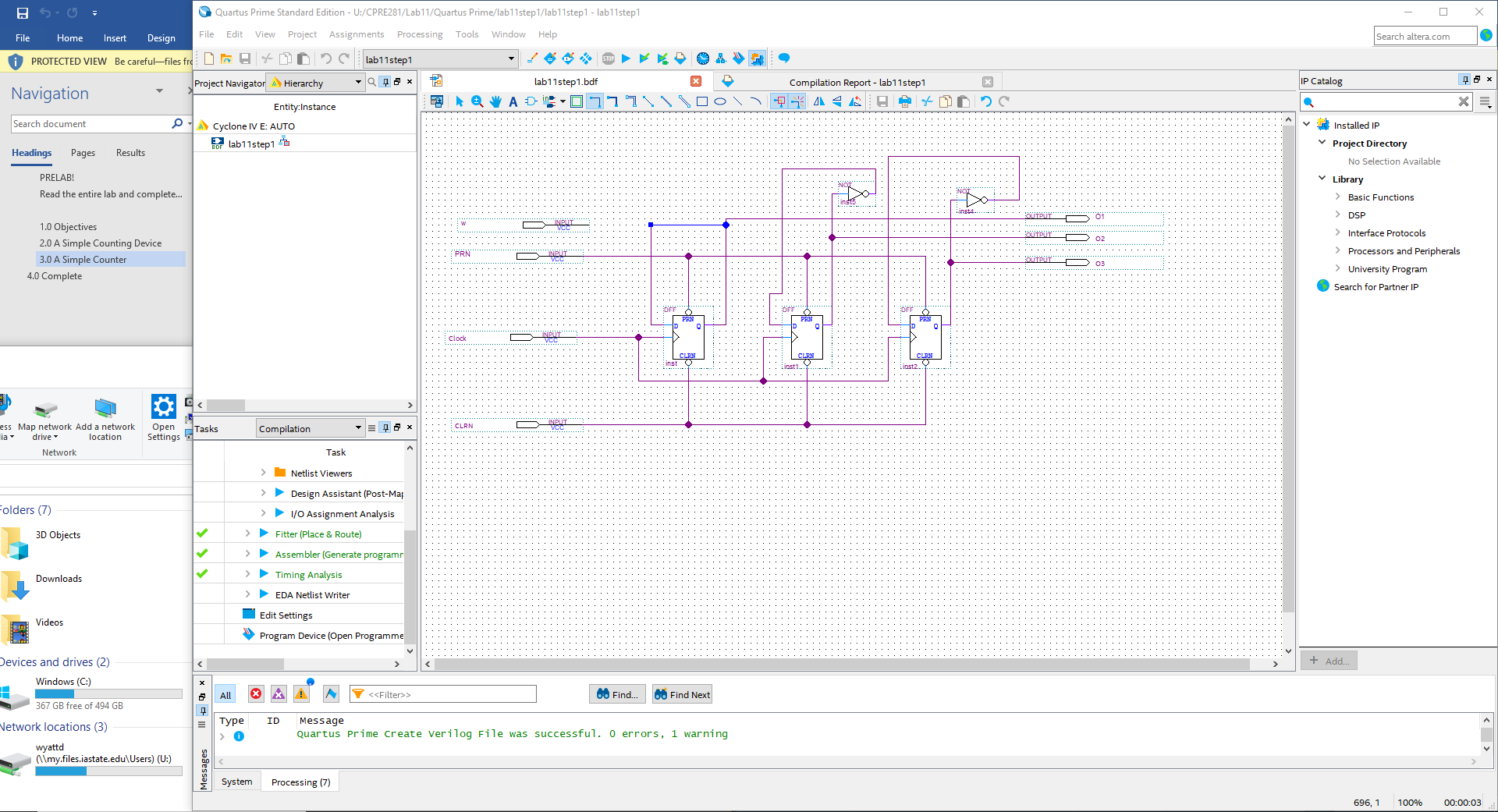
endmodule

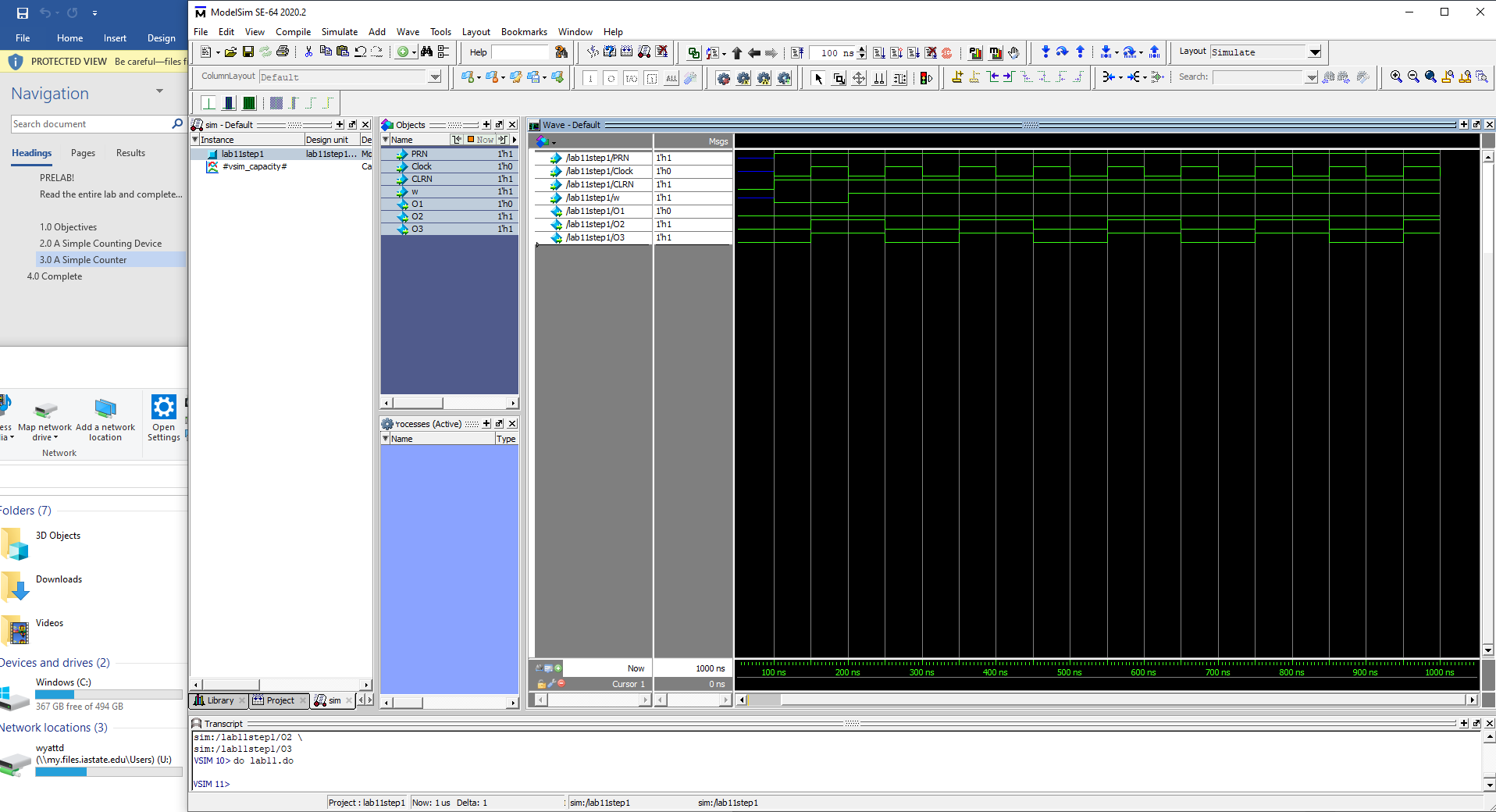
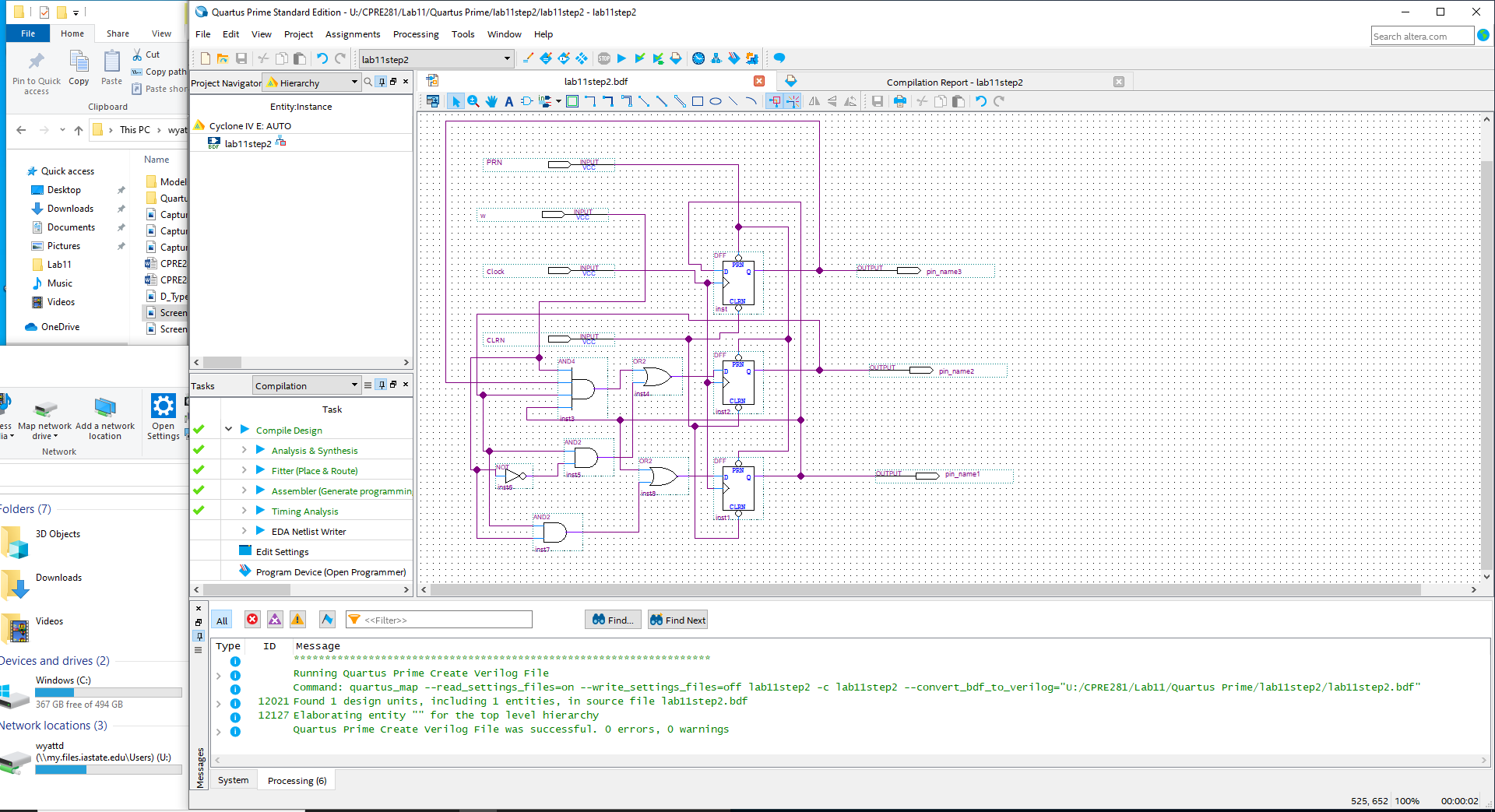
**LAB:**

**2.0 A Simple Counting Device**

Screenshots:

<<<Insert a screenshot of your module-6 counter BDF here>>>



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**3.0 A Simple Counter**

Screenshots:

